PoP Assembly (Package on Package) under Thermal Cycles

by

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http://nepp.nasa.gov

Outline

- **2.5/3D Advanced Packaging Technologies**
  - **Package on Package (PoP)**
  - System in Package (SiP)
  - Through Silicon Via (TSV)
- **PoP Assembly Configurations**
  - Daisy-chain PoPs
  - 4 types of assemblies, flux, 3 tin-lead, and 1 lead-free COTS
- **TC Reliability of PoP Assemblies**
  - Accelerated Thermal cycle, ATC, (-55°C/125°C), 4 configurations
  - Accelerated Thermal Shock Cycle, ATSC, (-100°C/125°C), two configurations
- **Non-destructive Evaluations to 1500 ATC Cycles**
  - Daisy-chain monitoring,
  - 2D X-ray,
  - Optical including scanning electron microscopy
  - 3D X-ray
- **Destructive Evaluation**
  - X-section verification of 3D X-ray images
- **Comparison to Literature on PoPs Reliability**
- **Summary**

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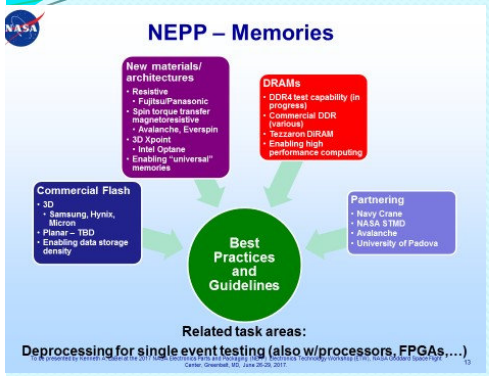
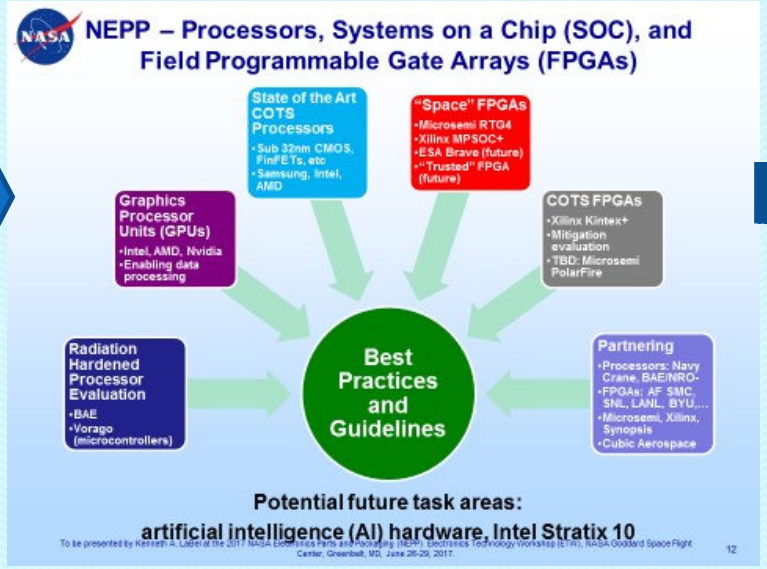
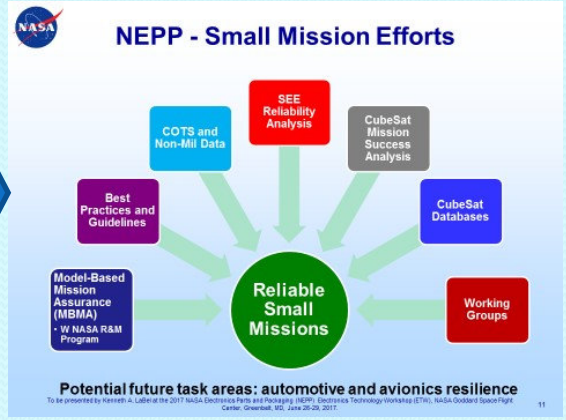
NEPP PoPs Reliability







Test PoPs Reliability

BOK Underfill

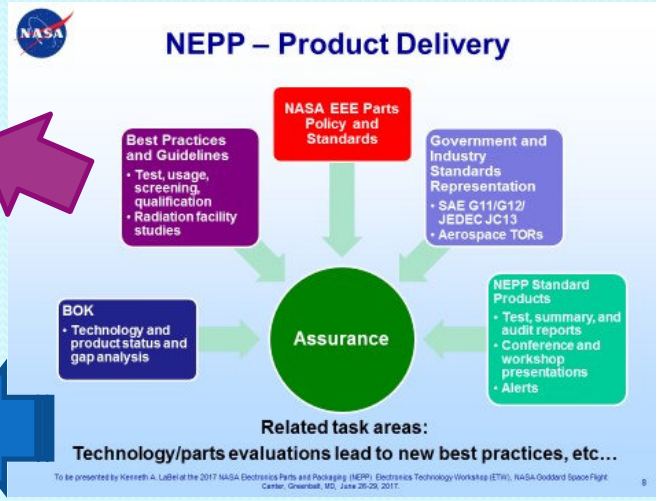
NEPP Website

Best Practices and Guidelines

- Test, usage, screening, qualification
- Radiation facility studies

BOK

- Technology and product status and gap analysis



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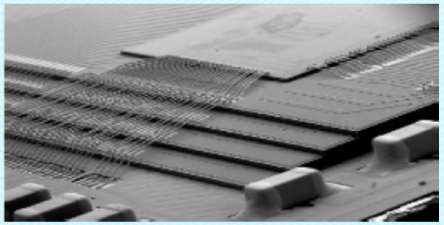
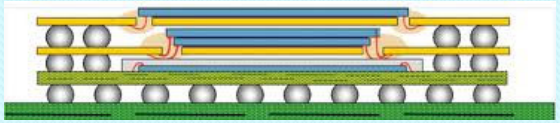
2.5D/3D Packaging Technology Trends

Stack Die
PoP/TMV

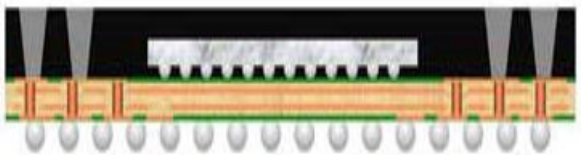
3D Wire Bond/Stack Die



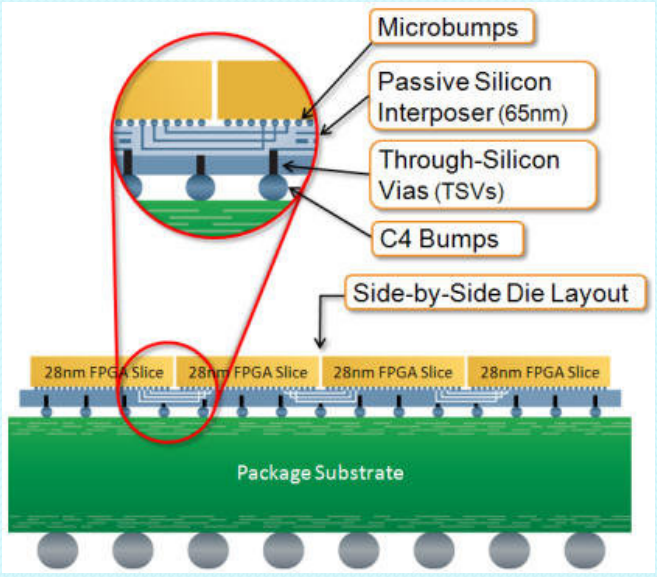
Package on Package (PoP)



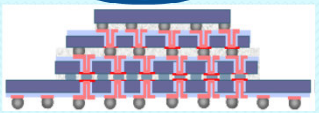
Through Mold Via (TMV)



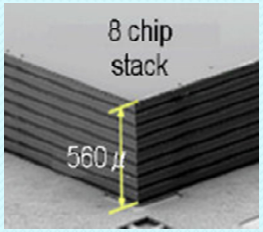
2D to 2.5 D
Single Chip to Multi-chip
TSV for Interposer



2.5D to 3DTSV
3D SIP

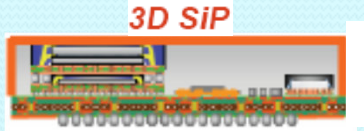


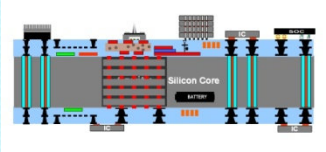
3D Wafer-level Packaging



Through-silicon Via

3D SiP





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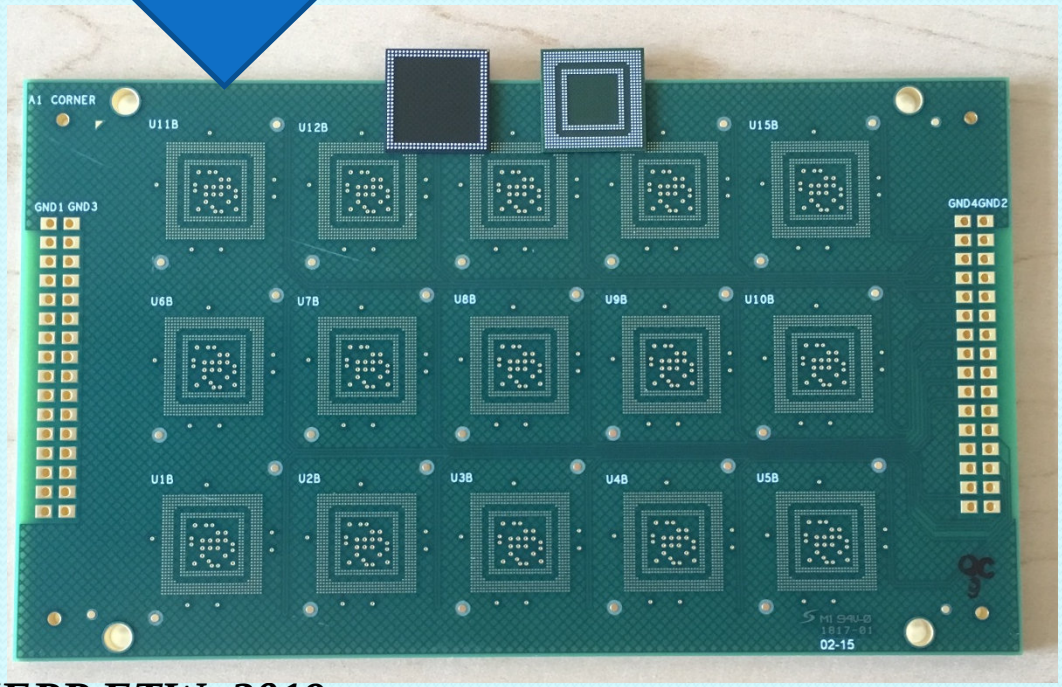
TMV/TSV Packaging
TV Methods

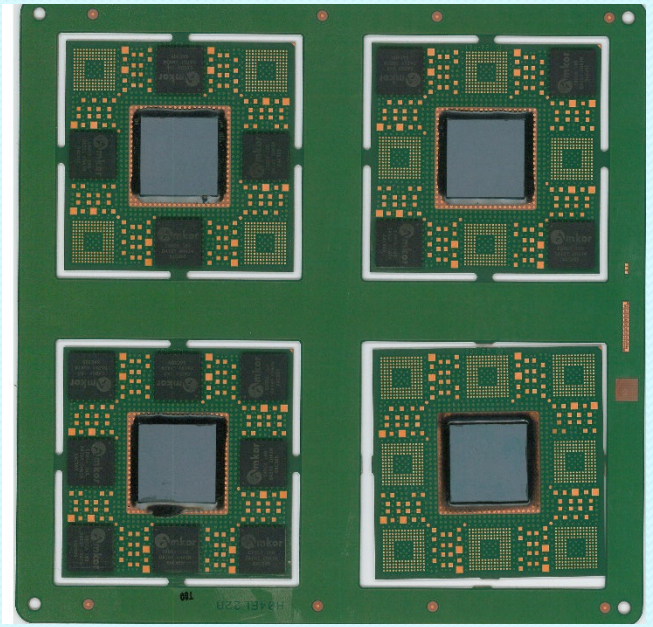
TMV

Through Mold Via (TMV)

2.5 D/ SIP

3D TSV





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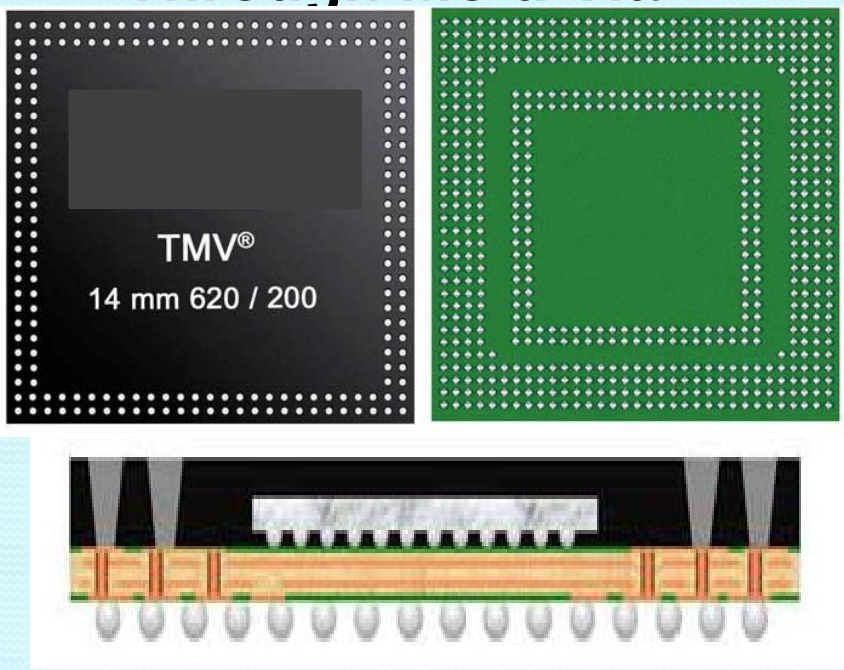
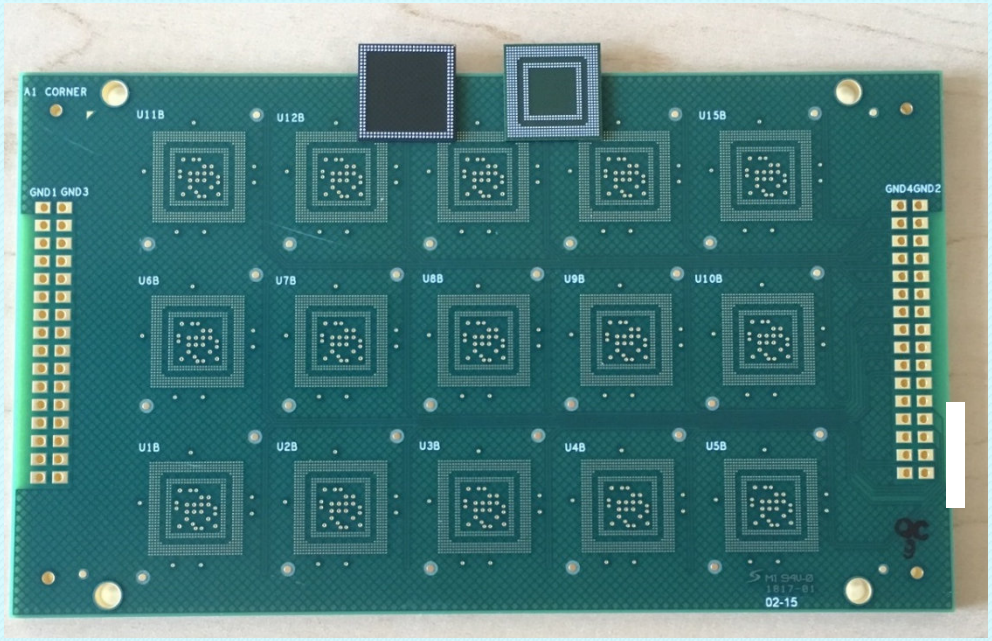
Package on Package TMV Evaluation

PoP

Through Mold Via





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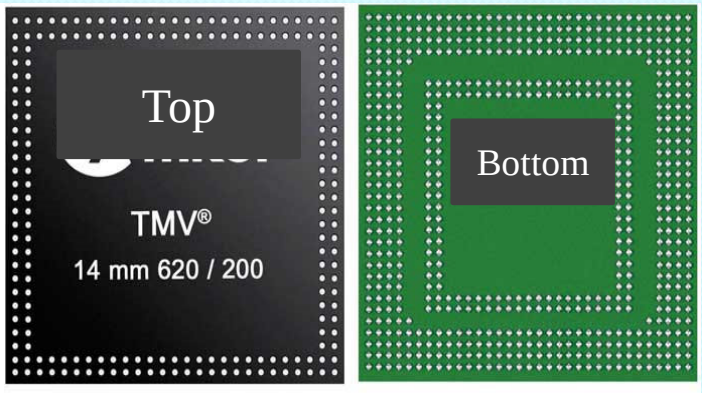
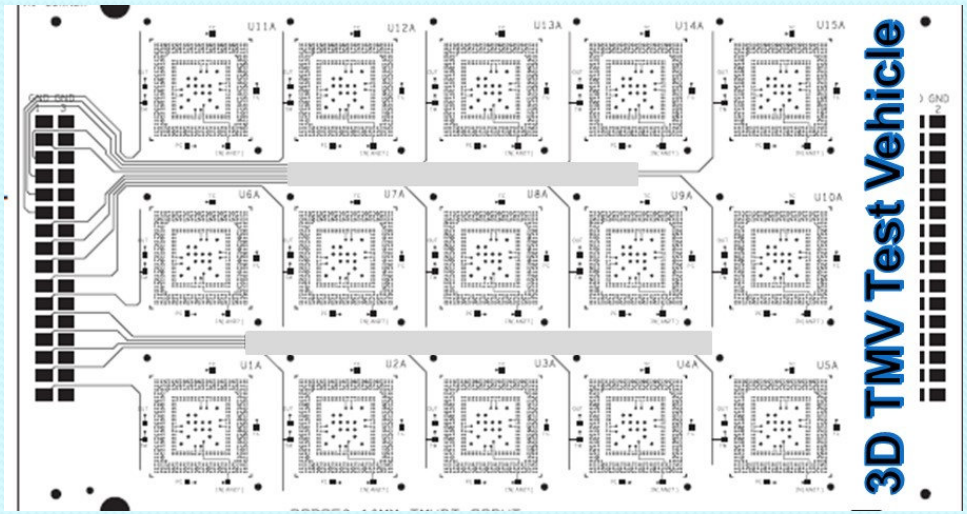
Daisy-Chain PoPs for Thermal Cycle

- ✓ DOE (design of experiment) technique for the effect of stack assemblies
- ✓ PCB material, FR-4 glass-reinforced epoxy laminate material, 93-mil (2.4-mm) thickness, microvia in pad, and electroless nickel immersion gold (ENEPIG) surface finish.
- ✓ The top package with 14 mm size had 200 lead-free tin–silver–copper ((98.5% Sn, 1% Ag, and 0.5% Cu), SAC105) balls with 0.5-mm pitch.
- ✓ The bottom FPBGA with through mold via package with 14 mm size had 620 balls of SAC125 (98.3% Sn, 1.2% Ag, and 0.5% Cu) with 0.4-mm pitch.
- ✓ Assemblies with lead-free solder covered the current COTS requirement
- ✓ Assemblies with tin-lead solder paste, backward compatibility, covered the high-reliability requirements.





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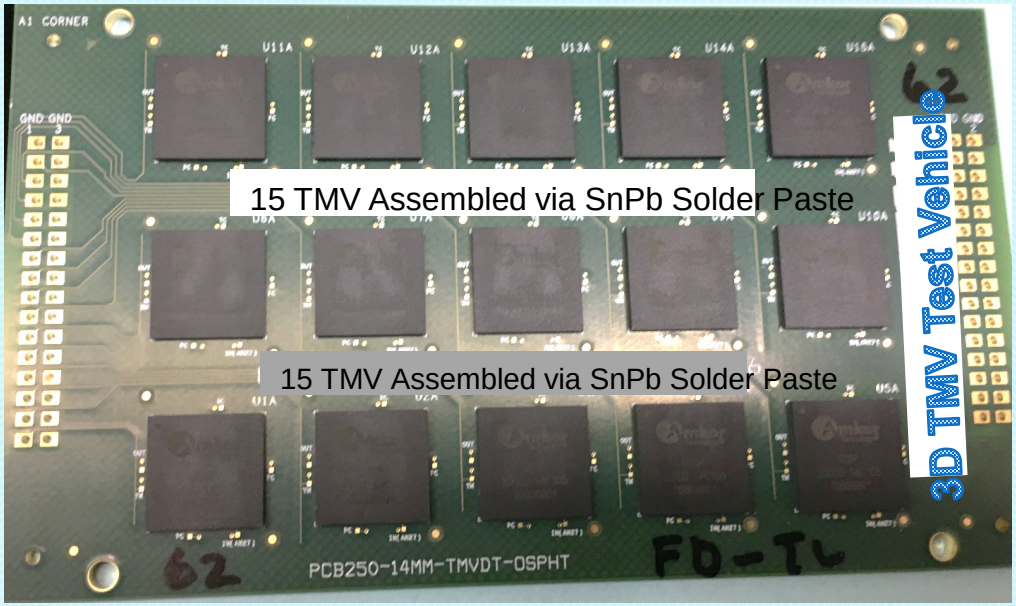
PoP Assemblies
Stacking During Assembly

- ✓ The top package was only fluxed and placed onto the lower package, which was placed on tin–lead (SnPb) solder paste (backward compatibility). Then, both were reflowed with 15 PoP packages (see Figure 4).
- ✓ Solder paste was placed onto the bottom package pads prior to placement of the top package, which was placed on SnPb solder paste of the PCB pad patterns (backward compatibility). Then, the TMV™ stacks were reflowed.
- ✓ Solder paste was placed onto the bottom package pads prior to placement of the top package, which was placed on SAC305 solder paste of the PCB pad patterns (lead-free assembly). Then, the PoP stacks were reflowed.



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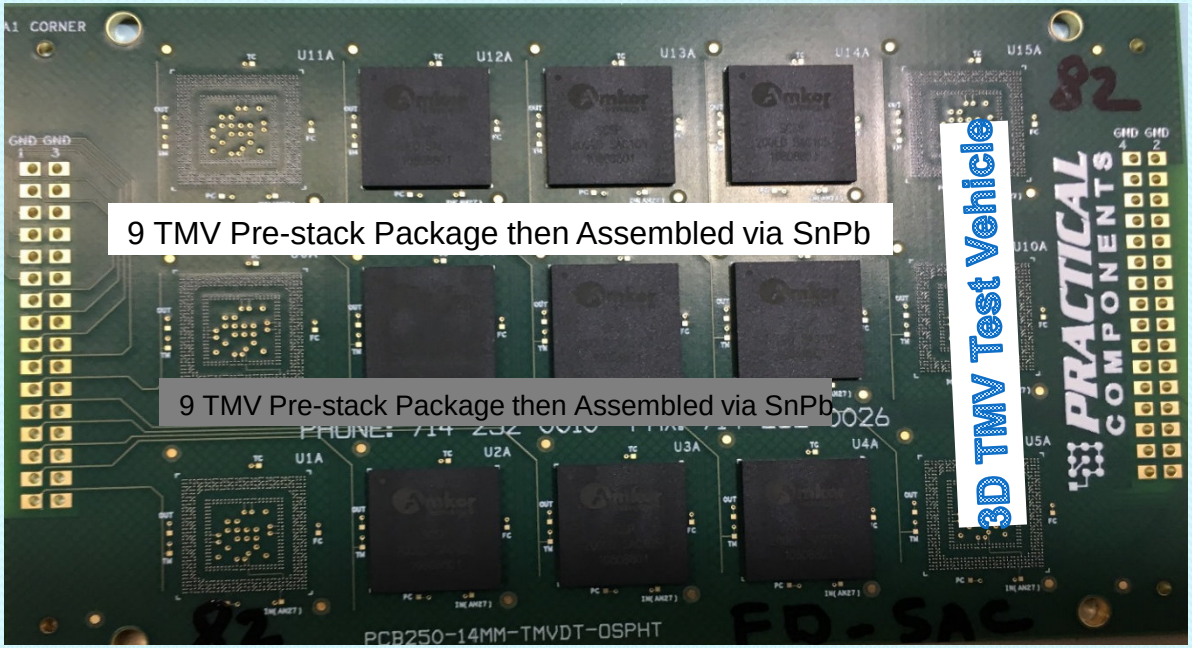
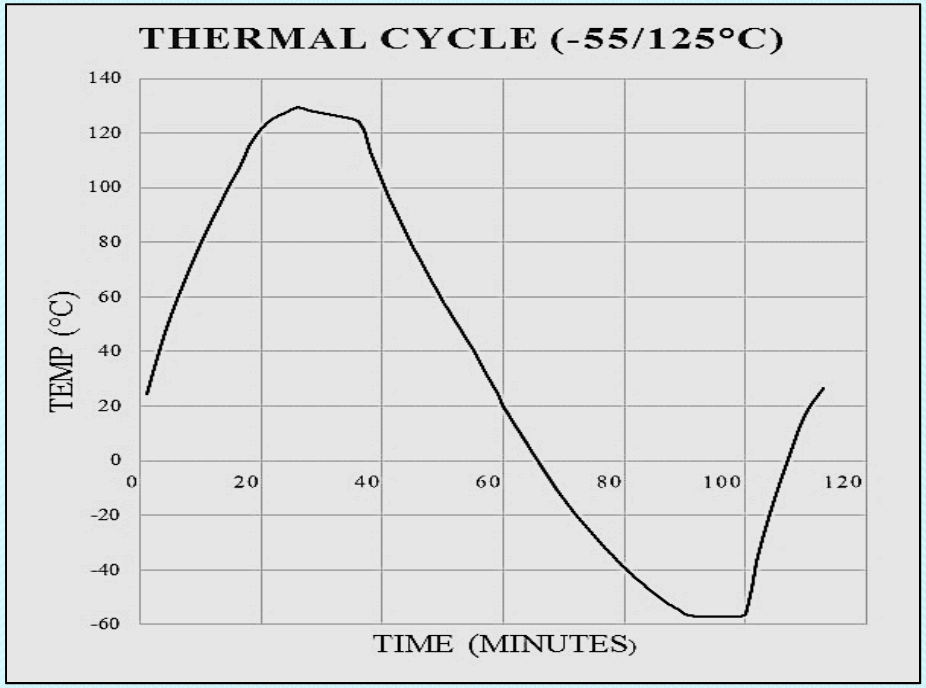
PoP Assembly
Pre-Stacked PoPs

- ✓ **Pre-stacked package as a unit with SnPb solder and then assembled the stacked package onto PCB with SnPb solder paste (backward compatibility). Then, the pre-stack reflowed with 9 PoP packages.**
- ✓ **The pre-stacked approach is possibly the most applicable approach for high-reliability applications even though this approach is the most costly and time consuming.**



PoP Assembly
Thermal Cycle Conditions

- ✓ Two different thermal cycling profiles: accelerated thermal cycle (ATC) or accelerated thermal shock cycles (ATSC).
- ✓ The ATC profile was in the range of –55℃ to 125℃ using a single chamber for cycling, with a slow ramp rate of about 5℃ and dwells of about 15 minutes with a total of 115 minutes.
- ✓ The ATC meets IPC 9701 for thermal cycling, it meets the ramp rate requirement of lower than or equal to 20℃/min.



PoP ATC Test Results

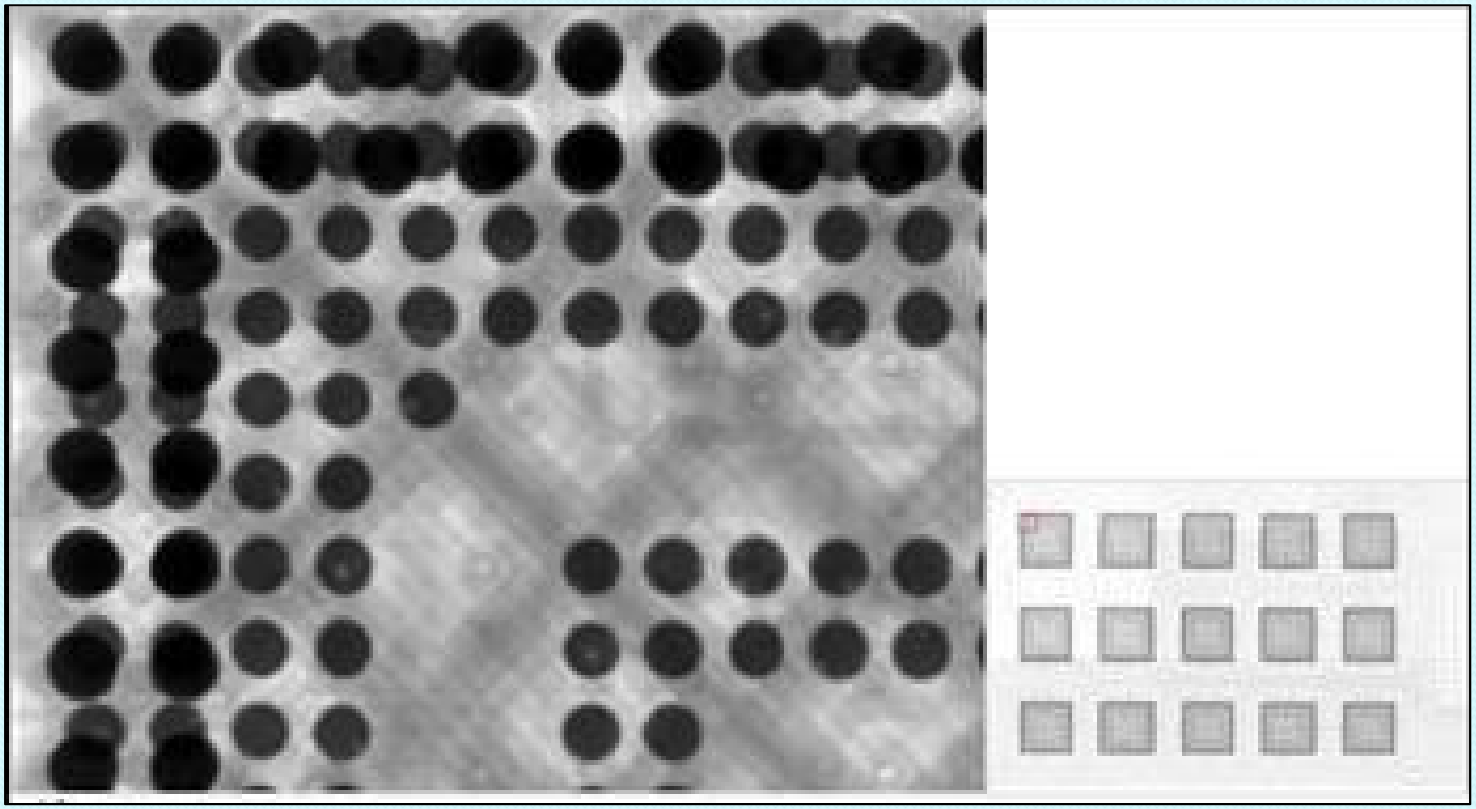
- ✓ **No PoP failures to 700 ATC, the limitation set by the pre-stack thermal cycles, late start in cycling. After 1500 ATC:**
- ✓ **SAC/SAC PoP assemblies showed 34% (3/9) failures**
- ✓ **SnPb/SnPb assemblies showed 57% (7/15), a slightly higher than SAC/SAC.**
- ✓ **Highest failures when only flux for the top PoP with the bottom package still soldered with tin-lead solder.**

Note that no distinguishing was made between the failures of the top or bottom package daisy chain, the PoP considered as one entity.

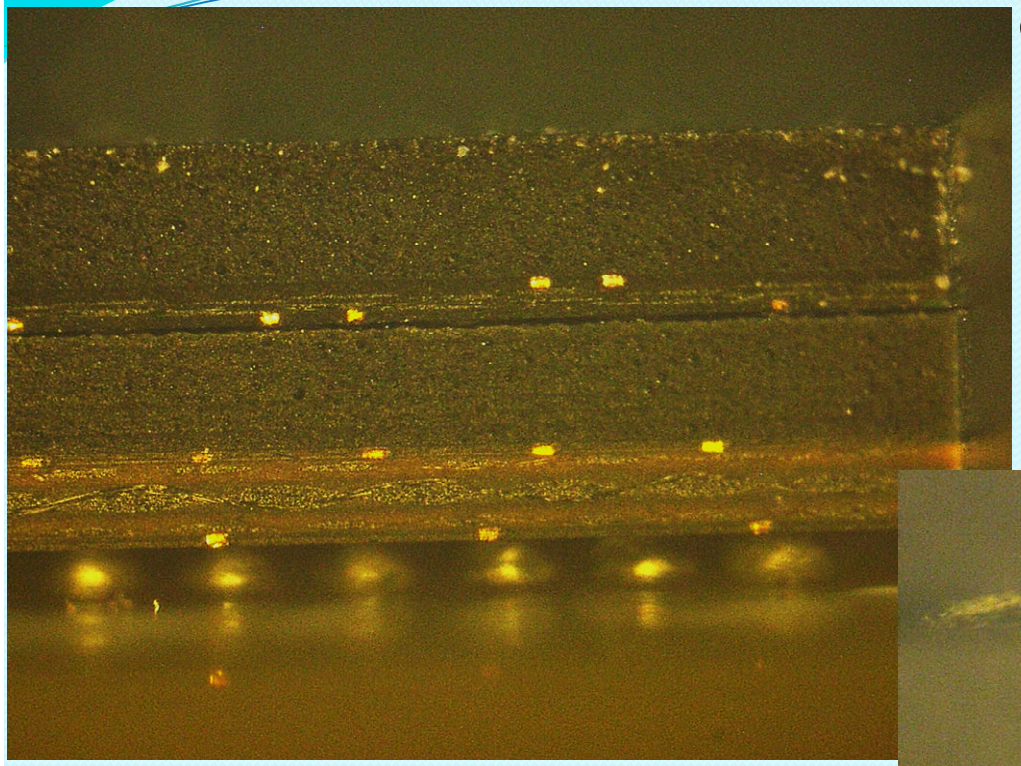
PoPs / Cycles	T: SAC305 B: SAC305 SN71, Failures Ratio	T: SnPb B: SnPb SN50, Failures Ratio	T: Flux B: SnPb SN61, Failures Ratio	Pre-Stack T/B: SnPb SN101, Failures Ratio
200	0/9	0/15	0/14	0/9
500	0/9	0/15	0/14	0/9
700	0/15	0/15	0/14	0/9
1100	0/9	0/15	4/14	NA
1300	1/9	2/15	8/14	NA
1500	3/9	7/15	10/14	NA

Non Destructive Evaluation
2D X-ray

- ✓ Daisy-chain resistance evaluation monitoring for failure detection
- ✓ Non destructive evaluation by 2D X-ray
- ✓ Non destructive evaluation by 3D X-ray
- ✓ Scanning electron microscopy (SEM) for the as-assemble PoPs, during and after ATCs.

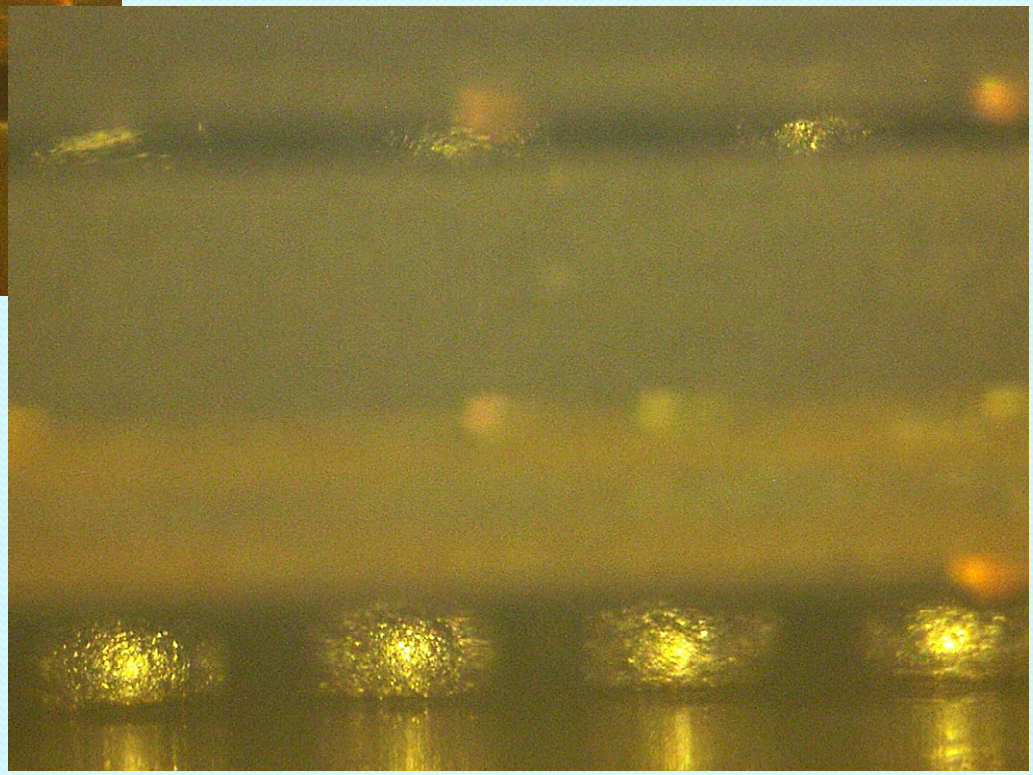


Optical Inspection after ATC



Bottom: Solder Paste
Top: Solder Paste

Bottom: Solder Paste
Top: Flux Only



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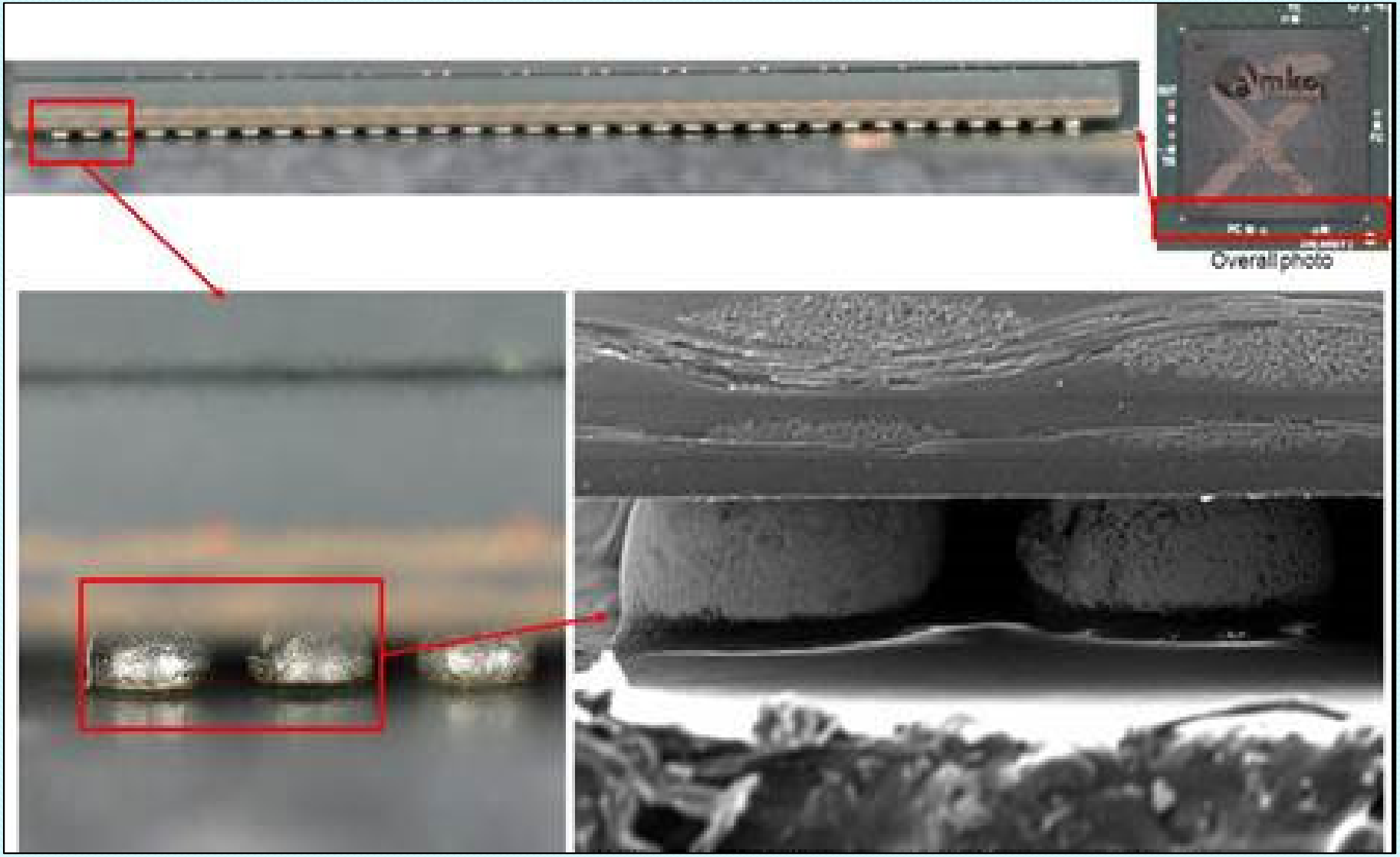
SEM Inspection after ATC



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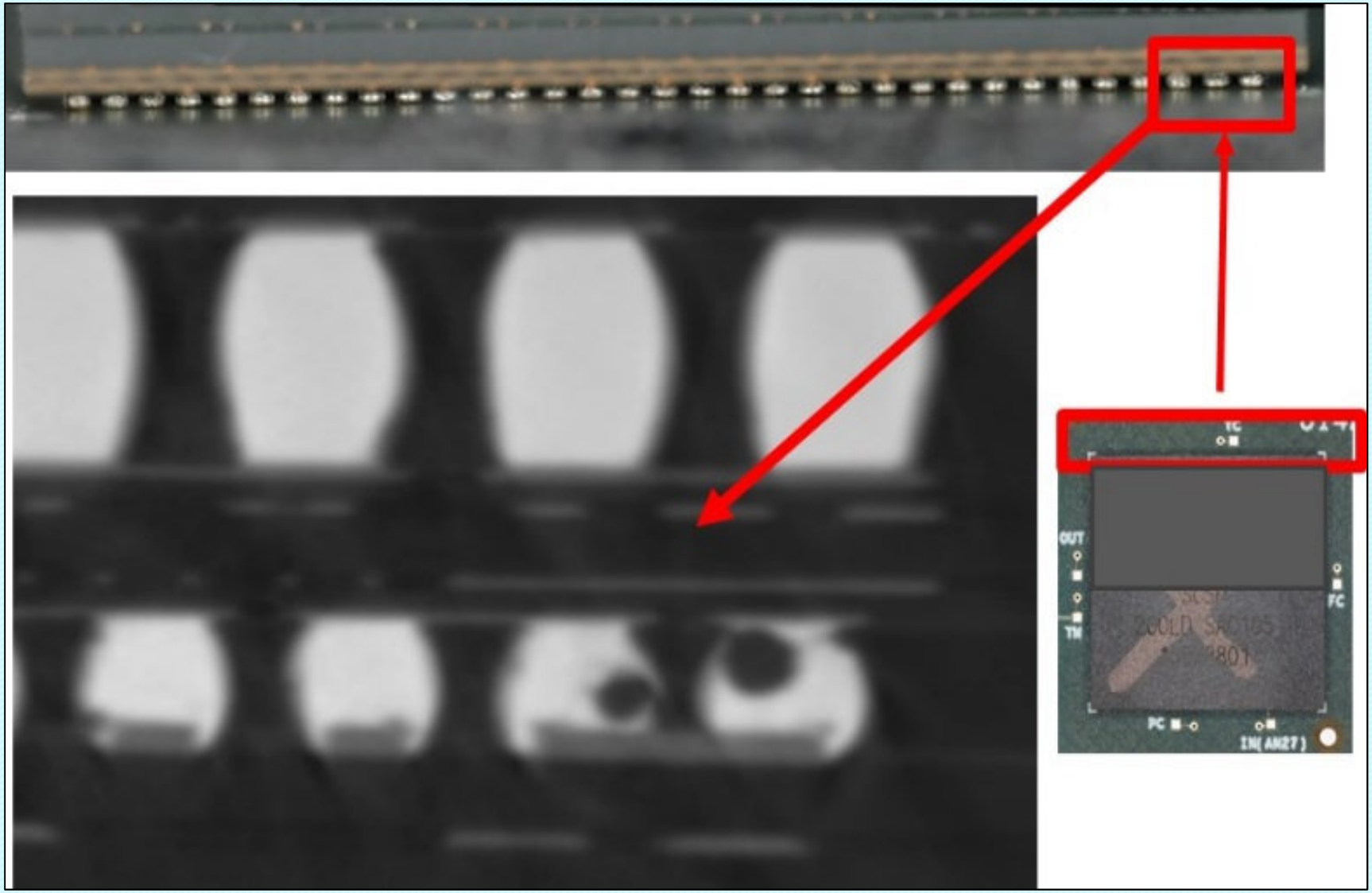
3D X-ray Inspection after ATC



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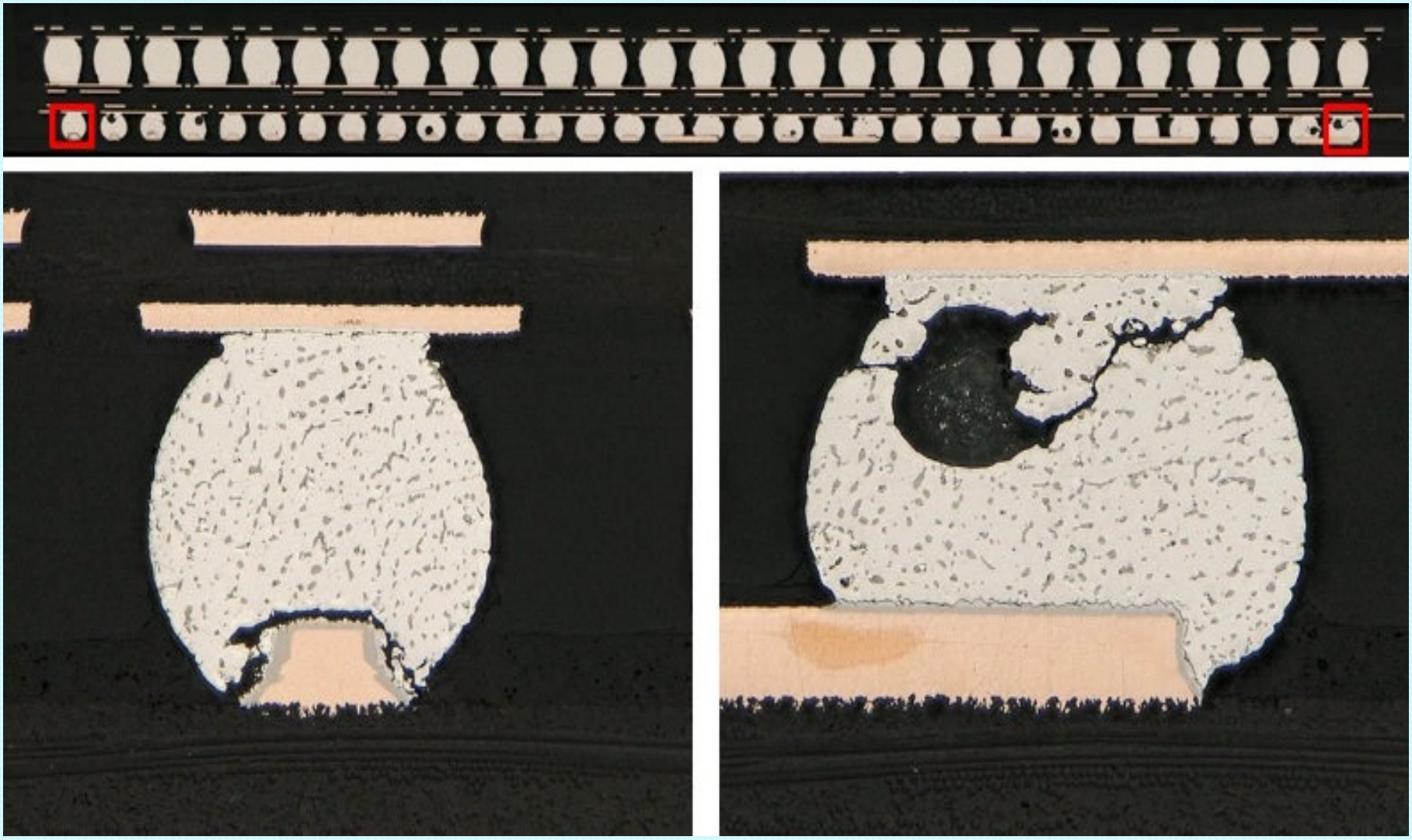
X-section Verified
3D X-ray Evaluation



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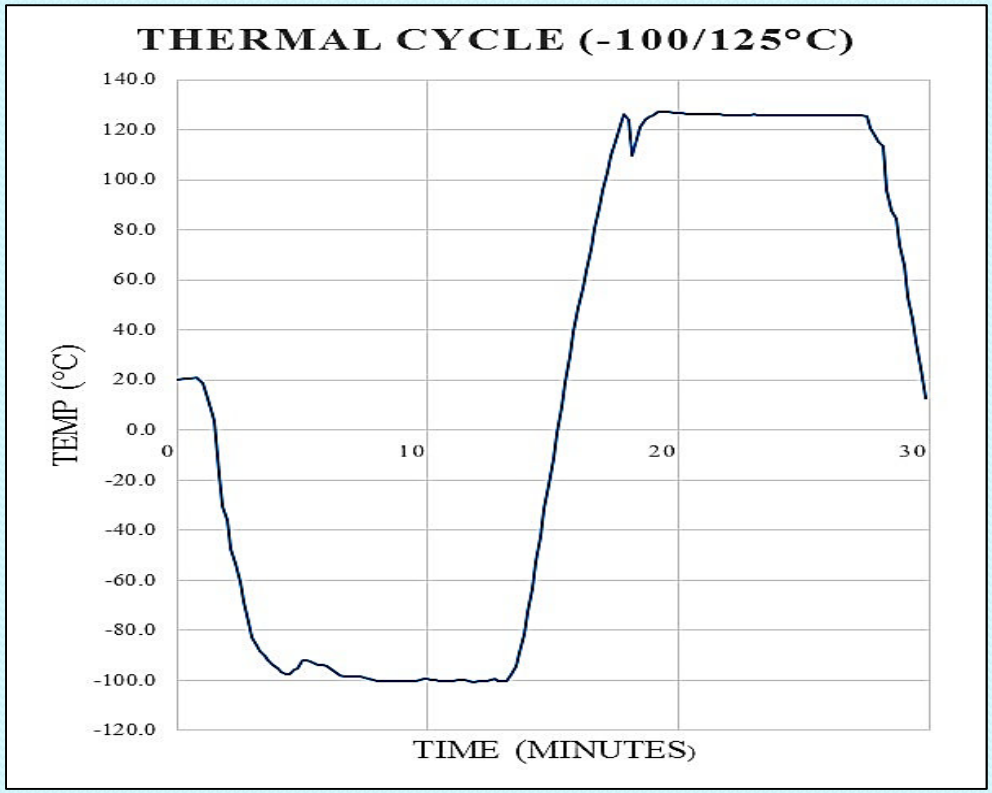
PoP Assembly
Accelerated Thermal Shock Cycle (ATSC)

- ✓ **ATSC (–100℃ to 125℃), using a single chamber with direct liquid-nitrogen exposure.**
- ✓ **Two PoP assemblies subjected to the ATSC.**
  - ✓ Lead-free solders at both the top/bottom, 9 PoPs
  - ✓ Tin-lead solders at both the top/bottom, 15 PoPs



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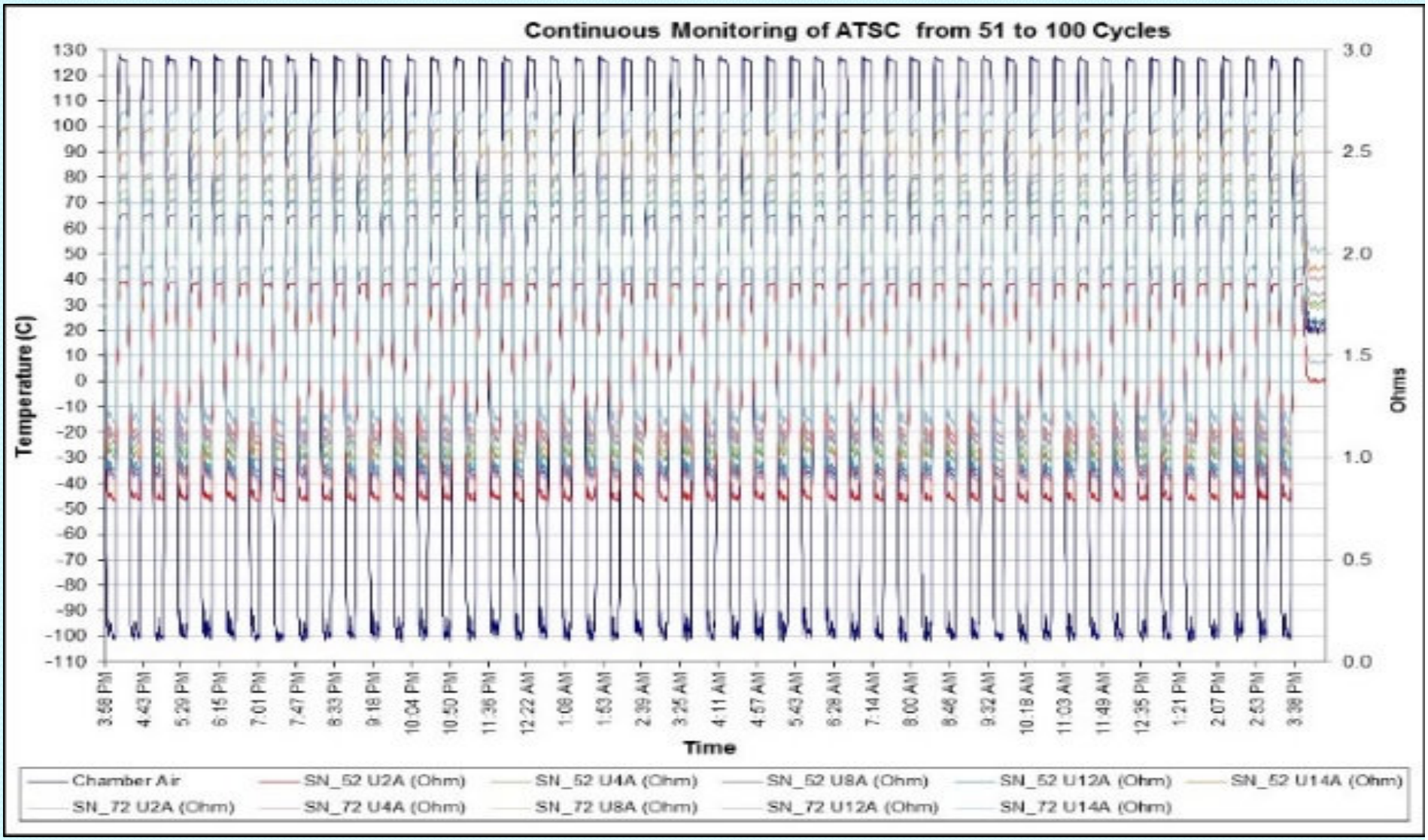
PoP Assembly

100 ATSC (-100°C/125°C) - No Failures



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Comparison to Literature

PoPs / Cycles	T: SAC305 B: SAC305 SN71, Failures Ratio	T: SnPb B: SnPb SN50, Failures Ratio	T: Flux B: SnPb SN61, Failures Ratio	Pre-Stack T/B: SnPb SN101, Failures Ratio
200	0/9	0/15	0/14	0/9
500	0/9	0/15	0/14	0/9
700	0/15	0/15	0/14	0/9
1100	0/9	0/15	4/14	NA
1300	1/9	2/15	8/14	NA
1500	3/9	7/15	10/14	NA

Underfill, Top	Underfill, Bottom	Range (cycles) Top	Range (cycles) Bottom	Crack Initiation* Top	Crack Initiation* Bottom
None	None	1400 – 1700		39000	1200

- P. Vianco et al. [25] presented Thermal cycling condition (–55°C/125°C, 15 min hold, 0– 7500 cycles).
  - **No underfill: The preference was indisputable for bottom joint failure.**
  - Underfill, bottom only: Top joints were preferred to fail first.
  - Underfill, both: Bottom joints were slightly preferred as first-failure.

[25] Vianco, P., Neilsen, M., Rejent, J., Grazier, J., Kilgo, A., "Predicting the Reliability of Package-on-Package Interconnections Using Computational Modeling Software," Proc. Surface Mount Tech. Assoc. Inter. 2013.

Underfill

- Released BOK on "Underfill Technology Assessment"
  - http://nepp.nasa.gov
- Section 4.1: Underfill Reliability for PoP/3D Stack Assemblies
  - Limited reliability test data
  - General agreement that: Trade offs between drop and thermal cycles need to be made
- Underfill for PoPs – Finite Element Analysis (FEA)
  - J. Xia et al. [24] FEA's analysis showed that underfilling reduced significantly the maximum stress for the bottom package, but had a minimum effect on the stress condition for the top package.
    - It was shown that the stress level of the bottom package approaches to the top package stress condition as filling condition increased from corner to edge and underfilling— the critical solder joint was no longer located at the bottom package for the underfilling condition.
    - Authors recommend that the corner-filling should be considered as the most cost effective approach for strengthening PoP to both mechanical and thermal cycling.

[24] Xia, J., Li, G. and Zhou, B., "Analysis of Board Level Vibration Reliability of Pop Structure With Underfill Material". In Electronic Packaging Technology (ICEPT), 2016 17th International Conference on (pp. 37-42). IEEE

Summary

- For an ATC of –55°/125°C, the four 3D PoP stack configuration assemblies— built with SnPb solder at package onto PCB with SnPb or flux at PoP level and pre-stack with SnPb on PCB as well SAC/SAC—did not show failures at 500 ATC determined by daisy-chain resistance measurement.
- For an ATSC of –100°/125°C, the two PoP tack configuration assemblies—built with SnPb solder at package/PCB and SAC/SAC at package/PCB levels — did not show failures after 100 ATSC determined by daisy-chain resistance measurement.
- Failure analyses performed on SnPb/SnPb PoP by optical/SEM, 2D/3D X-ray, and destructive cross-sectioning after 1500 ATC cycles showed that the key failure occurred at the bottom package with solder joint at package/PCB interfaces. Failure mechanisms for other PoP configurations yet to be determined.

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Thank You!

Reza Ghaffarian/JPL/Caltech